IN THE CLAIMS

1. (currently amended) A method of checking for errors in line width in an integrated circuit design, comprising:

identifying with a line width marker any lines having a line width greater than minimum line width;

associating a line width parameter with each line width marker, the line width parameter corresponding to a line width for the marked line; and

comparing the line width parameter for each line width marker with an actual layout line width.

2. (currently amended) A method of checking for errors in line width in an integrated circuit design, comprising:

identifying with a line width marker any lines having a line width greater than a minimum line width;

containing each line width marker in a line width layer;

associating a line width parameter with each line width marker, the line width parameter corresponding to a line width for the marked line; and

comparing the line width parameter for each line width marker with an actual layout line width.

3. (previously presented) The method of claim 1, wherein a layout that contains the layout line further comprises a component layer having components of the integrated circuit.

4. (original) The method of claim 1, and further comprising indicating an error when the actual layout line width is less than the line width parameter.

5. (original) The method of claim 1, and further comprising recording an error when the actual layout line width is less than the line width parameter.

6. (currently amended) The method of claim 1, and further comprising excluding checking for errors in areas of the integrated circuit ~~near or~~ above a connected transistor or in predetermined areas of the integrated circuit around an area of a connected transistor.

7. (previously presented) The method of claim 1, wherein the lines having a line width greater than a minimum line width comprise lines for carrying power to transistors of the integrated circuit.

8. (currently amended) A method of checking for errors in line width in an integrated circuit design, comprising:

defining a line width layer;

identifying with a line width marker any lines having a line width greater than a minimum line width;

associating a line width parameter with each line width marker, the line width parameter corresponding to a line width for the marked line; and

comparing the line width parameter for each line width marker with an actual layout line width.

9. (original) The method of claim 8, and further comprising indicating an error when the actual layout line width is less than the line width parameter.

10. (original) The method of claim 8, and further comprising recording an error when the actual layout line width is less than the line width parameter.

11. (original) The method of claim 8, wherein the line width layer contains each line width marker.

12. (currently amended) The method of claim 8, and further comprising excluding checking for errors in areas of the integrated circuit ~~near or~~ above a connected transistor or in predetermined areas of the integrated circuit around an area of a connected transistor.

13. (previously presented) The method of claim 8, wherein the lines having a line width greater than a minimum line width comprise lines for carrying power to transistors of the integrated circuit.

14. (currently amended) A method of checking for errors in line width in an integrated circuit design, comprising:

identifying with a line width marker any lines having a line width greater than a minimum line width;

containing each line width marker in a line width layer;

associating a line width parameter with each line width marker, the line width parameter corresponding to a line width for the marked line;

comparing the line width parameter for each line width marker with an actual layout line width; and

generating an error condition when the actual layout line width is less than the line width parameter.

15. (previously presented) The method of claim 14, wherein a layout that contains the layout line further comprises a component layer having components of the integrated circuit.

16. (previously presented) The method of claim 14, wherein the lines having a line width greater than a minimum line width comprise lines for carrying power to transistors of the integrated circuit.

17. (original) The method of claim 14, and further comprising indicating or recording the error condition.

18. (currently amended) A method of checking for errors in line width in an integrated circuit design, comprising:

identifying with a line width marker any lines having a line width greater than a minimum line width;

containing each line width marker in a line width layer;

associating a line width parameter with each line width marker, the line width parameter corresponding to a line width for the marked line;

comparing the line width parameter for each line width marker with an actual layout line width;

indicating or recording an error when the actual layout line width is less than the line width parameter; and

excluding checking for errors in areas of the integrated circuit ~~near or~~ above a connected transistor or in predetermined areas of the integrated circuit around an area of a connected transistor.

19. (previously presented) The method of claim 18, wherein a layout that contains the layout line further comprises a component layer having components of the integrated circuit.

20. (previously presented) The method of claim 18, wherein the lines having a line width greater than a minimum line width comprise lines for carrying power to transistors of the integrated circuit.